An open question - Will the properties of electromigration and thermomigration have an adverse effect on the future of asynchronous logic design?

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Abstract

The question is asked whether or not Electromigration and/or Thermomigration, phenomena that are both well known to cause the degredation of the physical structure of electronic circuits, will have serious consequences for the future research, development and application of asynchronous logic devices.

A non-rigorous answer to this question is presented that describes how the nature of asynchronous design, which in only performing useful work when processing actions dictate, will have the effect of causing temperature discontinuities to arise in that logic. This is precisely a factor that increases the rate at which electromigration and thermomigration effects are known to occur and therefore must have serious implications for the lifetime operability of asynchronous devices as opposed to equivalent synchronous machines.

A comparison is made between two hypothetical processors, one synchronous the other asynchronous, in order to support this argument.

Keywords: Asynchronous Logic, Electromigration, Thermomigration.

1 Introduction

Electromigration and Thermomigration are phenomena that are well known to have adverse effects on the atomic structure of materials. In this paper these phenomena are examined with respect to electronic devices with particular emphasis being placed on the changes to the physical structure that may become manifest within asynchronous logic circuits.

Any asynchronous circuit has the potential to operate within a wide range of operational environments, for example within widely varying temperature gradients and non-constant voltage supplies. As these factors are precisely the circumstances in which electromigration, *EM*, and thermomigration, *TM*, effects become prominent, the question is asked whether or not asynchronous logic design will ultimately be limited in scope and useability as compared to equivalent synchronous devices. This question becomes relevant when considered against the current drive towards the greater minaturisation of electronic devices especially as those devices will be likely to employ a greater current density flow which itself in turn increases *EM* and *TM* effects.

The remainder of this document will be taken up with a non-rigorous examination of the physical effects that may arise due to both *EM* and *TM*. This will be followed by a description of what is perceived to be the problem with asynchronous logic with regards to these effects together with a discussion as to whether or not asynchronous equivalent versions of synchronous devices will be likely to suffer from those same problems.

2 Electromigration

Electromigration is a well documented transport phenomena that is known to occur within solids [6] [7]. Essentially *EM* can be described as follows; In any electric field ions are subjected to a force due to that field and to a force which results from the motions of electrical carriers (electrons or holes). In bulk samples of solids (at very high temperatures, see section 3) these forces will cause the displacement of atoms by means of a lattice mechanism [5] which results in the diffusion of atoms across a material. When considering thin films, *EM* is known to occur at much lower tempertures (but at higher current densities) by a grain boundary diffusion mechanism. *EM* will also cause failures at material discontinuities such as at terminals, temperature gradients and at structural inhomogenities. In general failure times due to *EM* are a function of:

- the activation energy for diffusion
- the exponents of the current density

Electromigration is primarily a problem that is caused by dc currents with virtually no *EM* problems being caused by ac currents. When considering device lifetimes under both ac and dc currents it is true that a device will have a much longer lifetime if an ac current is utilised[1] but it must be noted that device failures will still occur under ac conditions [1].

If we now look at the mechanism of *EM* we can illustrate the process of atomic diffusion. In figure 1 we can see a lattice structure with a particular ion labelled at **A** and a hole at **B**.

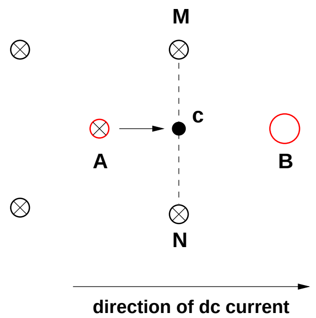

Figure 1: Diffusion action of an atom and a hole in a lattice structure.

[1]this is heavily dependant upon the current density.

Under the presence of a charge carrier, in this case electrons, the ion at **A** may move from left to right towards the direction of the hole. In order for this movement to occur **A** must pass between the atoms at **M** and **N** through the point **c**. This point at **c** is a non-stable equilibrium position (saddle point) such that if **A** reaches that point the ion will be just as likely to return to its starting position as it is to move towards the hole at **B**, e.g:

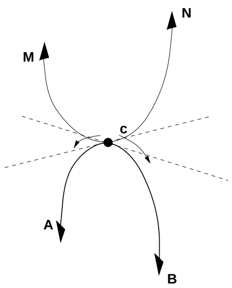

Figure 2: Non-stable equilibrium position in a lattice structure.

However though, under the continual electron bombardment[2] from a dc current, the probabilty that **A** will move towards the hole at **B** will be greatly increased, see figure 3(a). Under ac current conditions the electron bombardment factor is effectively ignored as there will be an equal "pressure" on an ion at **c** to move in either direction[3], figure 3(b).

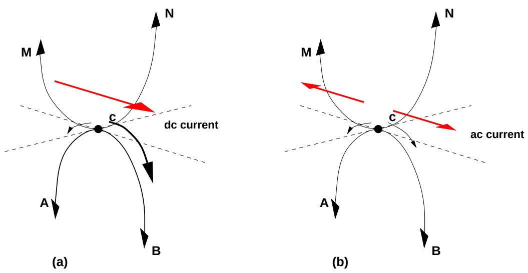

Figure 3: Electron bombardment conditions under ac and dc currents.

The net result of this process, under dc conditions, can be seen in figure 4. After a period of time there will be a gradual accumulation of ions in the area of a substrate that is in the downstream direction of that dc current.

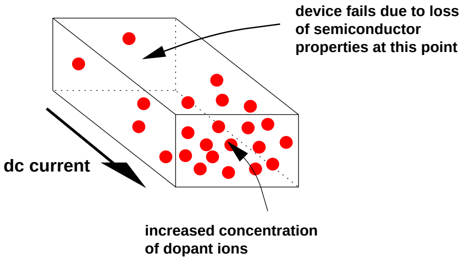

Figure 4: Ion accumulation due to a dc current supply.

[2]often referred to as the electron wind.

[3]this is basically why an ac current causes significantly less *EM* effects in a semiconductor device as atomic diffusion is just as likely to occur in one direction as it is in another thus averaging out the overall diffusion effect.

As transistor sizes of 0.1 micron and less are now being proposed there is the situation that as the dopants in such circuits are of such small quantities any alteration to the average distribution of those dopants will have a significant effect on the circuit performance.

Another factor which significantly contributes to *EM* in semiconductor devices is that due to material discontinuity effects which occur mainly at terminals[4].

At such places, where it is likely that two conductors joined together are made from different materials, there will be a disproportionate diffusion flow from one terminal to another, see figure 5(a):

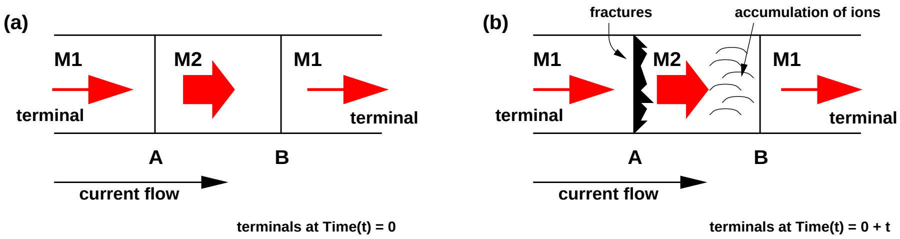

Figure 5: Transistor failure due to material discontinuity.

If the ions in material M_2 have a greater mobility than in M_1 there will be a gradual accumulation of material at discontinuity **B** with a corresponding depletion of material at discontinuity **A**, see figure 5(b). This will eventually lead to a physical rupture at **A** leading to device failure.

The aspects of device failure as described above have related specifically to circuits operating under a dc current. We can now show how such dc effects will manifest themselves in an electronic circuit.

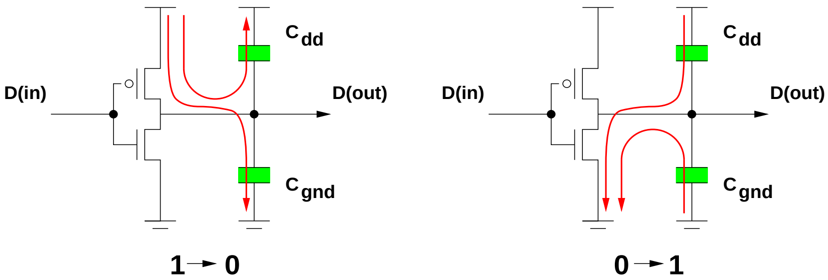

Figure 6: Uni-directional current flow through the transistors of an invertor circuit.

In the invertor circuit in figure 6 above we can see that when there is a change from the $1 \rightarrow 0$ state or the $0 \rightarrow 1$ state there is **uni-directional** flow of current through the transistors of that circuit. It is this uni-directional aspect of current flow that has a net result of there being *EM* and *TM* activity that will physically occur in those invertor transistors. This is a phenomenon that occurs in all electronic circuits.

[4]the material discontinuity factor tends to be a significant problem under dc current conditions only but is included here for completeness. This problem is more relevant to the thermomigration aspects as covered in section 3.

In the general case at low current densities and low temperatures electromigration will not be a significant cause of device failure. When *EM* does become a problem is when these conditions are relaxed, for example when fluctuations of temperature and/or current density occurs.

3 Thermomigration

Thermomigration is defined as *"the flux of mass induced by a temperature gradient"* [2]. The most efficient electrical conductors, which also tend to be the best thermal conductors, have electron transport as the means of heat conduction, whereas in poor electrical conductors thermal conduction will be due to a lattice vibration mechanism. Any electron, that has a temperature higher than the region into which that electron enters, will be diffused towards a cooler region almost as if a potential were acting upon that body. This *thermodynamic potential* gives rise to a thermodynamic force which is effectively a drift motion that is limited by the collisions of the electrons with obstacles.

Unlike electrical conductivity, where if an electron flows out of a region that electron will eventually be returned to that region due to an external circuit, in the case of thermal conductivity electrons must be conserved. At an initial temperature gradient there will be a net flow of hot electrons towards a cooler region. This will cause a concentration gradient that will cause an increase in the number of cool electrons that will diffuse back towards the hot region. This process will continue until a state of dynamic equilibrium is reached, see figure 7:

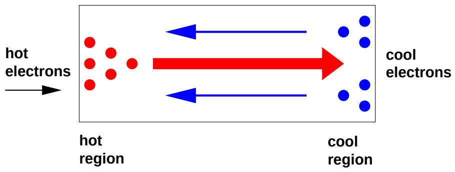

Figure 7: Dynamic thermal equilibrium.

If two regions in contact with each other are maintained at different temperatures mass transport can be observed to occur between those regions. This mass transport, known as the Soret effect, is also known as thermomigration and can be distinguished experimentaly from electromigration by performing experiments using both ac and dc currents.

As mentioned previously, a change of electron wind force along the length of a conductor will occur whenever two conductors made from different materials are joined together or when differing temperature gradients are maintained[5]. Any temperature change that has a minimal effect on the electron wind force will have a pronounced effect on ion mobility. This is due to the fact that the diffusion coeficient will increase with increasing temperature. In figure 8 below we can see how if a portion of a conductor is maintained at a higher temperature than the rest of that conductor, thermomigration effects will cause depletition of ions in the hot zone with corresponding ion accumulation downstream in the direction of the carrier motion.

[5]effective charge decreases with increasing temperature.

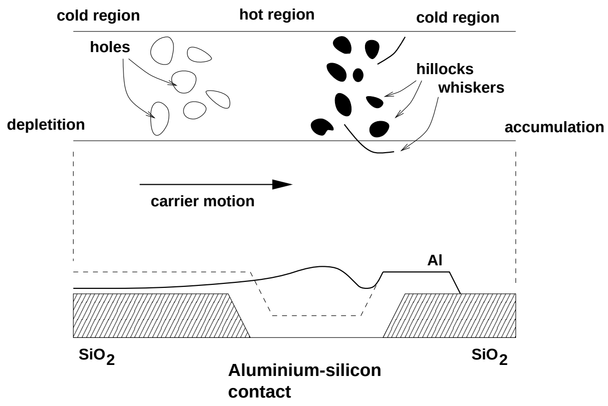

Figure 8: Temperature gradients across a conductor.

4 The problem with asynchronous logic?

In sections two and three we have shown how *EM* and *TM* influences can have adverse effects on the physical structure of electronic devices. In this section we will examine how such influences may manifest themselves with regards to both synchronous and asynchrnous digital circuits and we will put forward a proposal to suggest that asynchronous logic may be likely to suffer from these effects to a much greater extent.

There are many reasons why designers are now proposing that asynchronous logic is the next step forward in digital circuit design but for the purpose of this discussion we are only interested in the following main argument;

- **low power:** A typical synchronous circuit will employ a global clock which means that the majority of that circuit will be active at all times. The continual decrease in CMOS process rules has meant that modern CMOS logic has become much denser and faster to the point where modern microprocessors can be expected to dissipate 20 to 30 watts of power. With the current trend towards even greater miniaturisation these problems of power dissipation will continue to increase. The lack of a clock in an asynchronous circuit means that only those parts of the logic that are requested to perform any processing actions will be powered. Asynchronous logic design therefore tends to be inherentely "low powered" in aspect.

In the first instance let us consider two microprocessor circuits, both of which are designed to be equivalent devices. One of these structures is synchronous, by which we mean all processing actions will be regulated by a signal that has a fixed periodicy of operation, e.g. a "clock" and the other is asynchronous in which all processing actions will be performed when a relevant section of logic receives a signal which essentially says "start processing now". The general layout of our processors can be seen in figure 9 below:

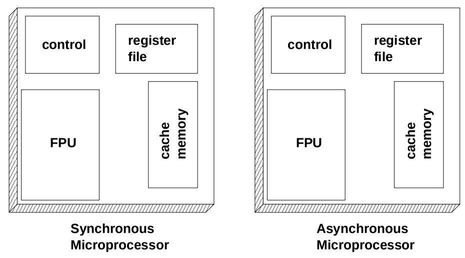

Figure 9: Equivalent synchronous and asynchronous microprocessor devices.

Other factors which are pertinent to the design of asynchronous logic, but not synchronous logic, which may be a cause for concern regarding *EM* and *TM* effects can now be described as the environments in which our processors above may be expected to operate may be likely to suffer from these same effects. Asynchronous logic has the advantage of having proven demonstrators that can and will operate in both variable temperature environments and under fluctuating/variable power sources [3] [4] [9]. It is these latter two facts that whilst having been demonstrated to be advantageous to asynchronous logic are in actual fact a cause for concern specifically with regards to device operational lifetimes.

Let us now consider two cases of operational environments for our two processors. The first case will involve constant ambient temperature and power supply whilst the second will involve both changing ambient temperature and power supplies.

4.1 Constant temperature and current supply

In this environment when our two devices are first switched on both *EM* and *TM* effects will be initially observed in both devices due to powering up mechanisms, resetting of logic, latches etc. Before we require our circuits to perform any processing actions we wait a period of time for both devices to reach their operational temperatures which we can see below if we look at the two temperature maps of the surface area, figure 10.

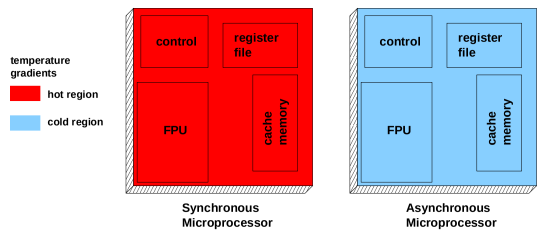

Figure 10: Operational temperatures of both processors.

Immediately we can see that the temperature of the two processors is not the same. The synchronous device will likely operate at a much higher temperature due to the fact that the synchronous clock will be continually in operation even though no useful actions are being performed (the clock is continually active in our example). We then request our devices to carry out the execution of a task, which does not require the use of the FPU unit, and then after a period of time we again look at the temperature of the surface area of our devices, figure 11;

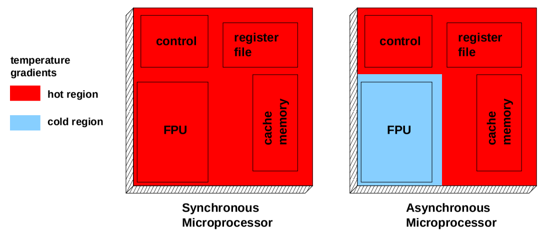

Figure 11: Temperatures of both processors after a period of sustained work.

We can now see how an asynchronous circuit is implicitly low powered as only those areas of the processor that are active will be powered and this is shown by the differing temperature regions across the surface of the device. Note that the synchronous processor is unlikely to have significant temperature changes after processing due to the fact again that the clock signal will ensure that enough transitions will occur to keep the temperature constant.

Both processors are now given different tasks to do. These tasks involve the use of the FPU but only to the extent of about one in ten instructions actually use that unit. If we then re-examine the temperature maps of our devices we again see how there is a constant temperature gradient within the asynchronous unit across which useful work is actually being performed. The overall temperature of the FPU does not increase significantly as there is not a sustained period of activity in this area.

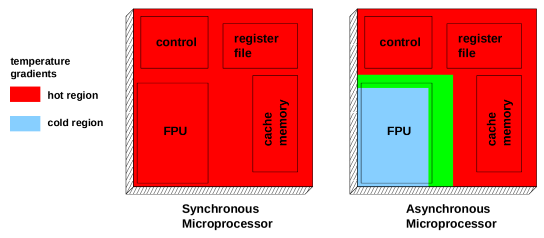

Figure 12: Temperatures of both processors after a period of sustained work involving the FPU.

This is the point where we see the percieved problem with asynchronous devices with regards towards *EM* and *TM* effects. At the temperature gradient near the FPU there will be significant thermomigration effects that will be observed in the logic that bounds that area, see figure 13:

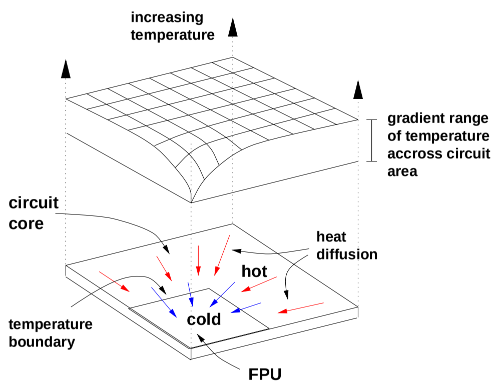

Figure 13: Surface temperature map of an asynchronous circuit showing thermomigration effects.

These problems do not occur within the synchronous device and as *EM* and *TM* can significantly reduce the MTBF figure of a circuit the conclusion must be drawn that if we are considering the overall lifetime of both our asynchronous and synchronous devices intuitively the lifetime of the asynchronous device must be less than that of the synchronous circuit. At any position in a device in which there are temperature gradients, thermomigration aspects will occur and which will ultimately degrade the semiconductor properties of the affected transistor areas. This problem can be summarised in the following hypothesis;

Hypothesis 1 *An asynchronous circuit that operates in an environment that has both a constant temperature and voltage power supply will have regions of circuitry across that device that will have differing temperatures. The boundaries between these regions will see enhanced electromigration and thermomigration effects take place that will significantly decrease the functional lifetime of that device.*

This does not bode particularly well for the employment of asynchronous logic as a replacement for equivalent synchronous designs. As both environmental trends and consumer requirements are becoming more focused on low power devices, asynchronous logic would seem to be well positioned to exploit and fulfill those needs. Unfortunately though consumers are not likley to be attracted to a product that will require more frequent replacements. Does this therefore mean that the drive to gain more acceptance of asynchronous logic will stall especially when we consider that there may be limited situations when an asynchronous device can succesfully replace a synchronous equivalent? In order to determine this we must first look at the second of our environmental situations in which our two hypothetical processors may operate.

4.2 Variable temperature and current supply

In this environment both processors will be expected to operate under conditions of fluctuating temperature changes and variable power supplies. The actual types of environment that we are considering here could translate to microgravity conditions, e.g. satellites, nuclear power stations, military applications etc. in essence any situation under which the operational working specifications of a device are exceeded.

When considering many of the modern synchronous microprocessor devices that are fabricated today we see that the working environmental specifications of these designs tend to be within narrow margins of operability, for example the Intel Pentium Processor (60/66 MHz model) has a working case temperature of 85^oC that is designed to restrict the surrounding ambient air temperature to a range of 40-45^oC [8]. Typical voltage requirements of these devices are within the range of 3.3V $\pm$ 0.2V. The previous values are typical of the constraints that modern synchronous devices are expected to operate under but it is to be noted that this does not compare very favourably to asynchronous devices that have been demonstrated to have much wider tolerances to changes in operational conditions. The TITAC processor [9] for instance, has an operational voltage of 5V but has been tested to work without error over a range of 2.5 to 7V. This is an order of magnitude greater of an operational constraint value.

Such synchronous processors as described above may not fare very well in environments which experience fluctuations in opertational conditions and in many cases it may be likely that such a device will not function at all. An asynchronous device on the other hand may continue to function under such fluctuating conditions but may have a much reduced lifetime of operation.

Consider the following situation: Our asynchronous device, designed to work at say 3V, may be affected by an irregular power supply. This power supply may vary by several volts over time and so it must be that case that the device will experience greater temperature changes across the complete circuit due to the different rates of current density supplied. This of course will have a much greater impact when electromigration and thermomigration effects are considered as extreme temperature changes will enhance that rate at which such EM and TM effects occur. On the other hand our synchronous device, also designed to operate at 3V, when faced with a 5 or a 6V supply, may cease to function altogether. The point of this argument is to state that under fluctuating operational conditions the asynchronous device will be likely to continue functioning whilst the synchronous device may not. This leads us to our second hypothesis;

Hypothesis 2 *An asynchronous circuit may be best suited to operate in an environment that has both a fluctuating temperature and voltage power supply. The operation of such a device under such conditions will be likely to cause that circuit to have regions across that device that will have large differing temperatures. The boundaries between these regions will see greatly enhanced electromigration and thermomigration effects take place that will significantly decrease the functional lifetime of that device.*

4.3 How significant will these EM and TM effects really be?

The next question to be asked is whether or not these EM and TM effects are really likely to be a significant factor when considering the lifetime of any digital circuit be that device synchronous or asynchronous. Using our two processors as defined earlier let us consider their projected 'theoretical' lifetimes in the following graph:

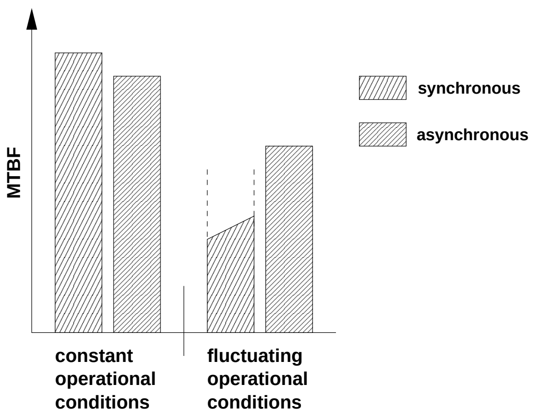

Figure 14: Projected theoretical lifetimes of our synchronous and asynchronous processors.

We can see clearly that under normal working conditions we would expect our synchronous processor to have the longest operational lifetime whereas in abnormal working conditions the asynchronous processor may prove to have the longest life. But will this actually be the case? The biggest factor which may override any such effects will be due to the actual process of manufacture of such devices. It may be the case that such factors as:

- lack of temperature uniformity during film deposition
- non-uniform doping
- introduction of impurities

and other such aspects may have the overall effect that the actual working lifetime of such devices may be significantly below the time period that must elapse before *EM* and *TM* effects will become significant. In the following graph we can see for example how the projected manufacturers lifetime of our devices may be well below that of the actual lifetime as limited by *EM* and *TM* effects.

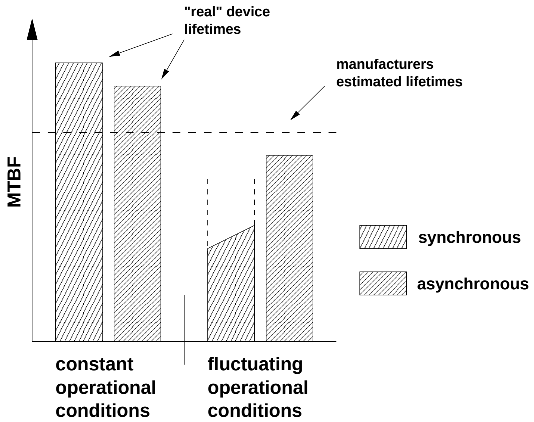

Figure 15: Manufacturer projected processor lifetimes.

The conclusions that would have to be drawn from the previous graph would be that if the projected operational lifetimes of both our asynchronous and synchronous processors were the same then the asynchronous device would have to be employed as the processor of choice due to all the advantages of being low powered, tolerant to environmental conditions etc. We could assume that the problems related to *EM* and *TM* would never become significant issues where device lifetimes were to be considered and in cases where such devices were to be employed in hostile environments it may be that only the asynchronous devices would function correctly anyway.

Another heating factor also to consider would be the working temperatures that such devices may be expected to function at. We again consider the Intel Pentium 60/66 MHz. processor with a maximum case operating temperature of 85°C. If our asynchonous equivalent device has a similar high working temperature, might it be the case that thermal diffusion throughout all the die materials of that asynchronous device would be enough to cancel out any local temperature discontinuity regions anyway. This would of course depend upon the thermal conductivity of the materials of that processor die but if this was the case then the overall effect would be to reduce the *EM* and *TM* activity in that circuit.

5 Conclusions

We have seen intutively how asynchronous circuits must suffer from electromigration and thermomigration effects to a greater degree than equivalent synchronous devices up to the extent that the lifetimes of such asynchronous circuits may be significantly reduced. It may be that case that such effects will never be significant when considered against all the other factors that determine the physical lifetimes of such devices. Asynchronous logic design is still an important field of VLSI and microelectronic research and it is true that such logic has many specific roles to play with regards to specific types of operational environment.

Further research and modeling of *EM* and *TM* aspects must be carried out in order to determine whether or not these problems are likely to have such a specific impact on the useability and general future of asynchronous logic design.

6 Acknowledgements

Acknowledgements must be made to several people whom acted as a sounding board for some of the ideas as expressed in this paper, specifically Alex Yakovlev, Albert Koelmans and Justin Pearson[6]. Specific mention must be made of Keith Heron who provided several insights into the nature of atomic diffusion, electromigration and thermomigration effects and who also reviewed the early drafts of this paper.

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